Improved RF capability and projected increase in die size [1] for CMOS circuits lead to the concept of wireless communications within and between chips. A potential application is wireless clock distribution, proposed as an alternative interconnect system capable of distributing high-frequency signals at the speed of light using microwaves [2]. The wireless clock distribution system consists of a clock transmitter, located on or off chip, broadcasting a microwave global clock signal at frequencies greater than 15GHz, and a grid of integrated clock receivers. Figure 19.6.1 shows a block diagram of a clock receiver. The global clock signal is received using an integrated dipole antenna. The signal is then amplified using a low-noise amplifier (LNA), frequency divided down to the local clock frequency, buffered, and distributed to provide local clock signals. This IC operating at 7.4GHz, which integrates antennas and necessary receiver circuits in 0.25µm CMOS with five metal layers on p-substrates, is a first step towards realizing such a system.

The antenna is a 2mm long, 10µm wide linear dipole [3]. In oxide (ε_r=3.9), 2mm corresponds to ~3/10 at 7.4GHz. The antennas are fabricated in metal 5, separated from the substrate by ~7µm of oxide. Figure 19.6.2 shows a schematic of the LNA and a source-follower buffer. A fully-differential topology rejects common-mode noise (such as substrate noise) eliminates the balanced-unbalanced conversion between the antenna and LNA input, and provides clock signals with 180° phase difference to the frequency divider. Each half-circuit of the LNA consists of a cascode amplifier with inductive source degeneration (L_s), a series inductor at the input (L_i), and an inductive load (L_d) [4]. The input of each half-circuit is matched to 50Ω.

Following the LNA are source-follower buffers. These buffers shift the DC level from the output of the first stage to the input of the divider, and help to isolate the capacitive load of the divider input from the tuned load of the LNA. A source-follower driving a capacitive load can have negative input conductance, proportional to the transconductance of M. This negative conductance is used to enhance the gain of the LNA by increasing the Q of the resonant circuit at the drain nodes of M. However, too much negative conductance can result in unstable operation. By adjusting the current through the source-follower, the gain can be improved while maintaining stability.

Figure 19.6.3a shows the measured S-parameters of an LNA without the source-follower buffers. The outputs of this LNA are matched using on-chip capacitive transformers [4]. Driving 50Ω, the LNA provides ~10dB gain with input and output reflection coefficients <15dB, consuming 211mW from a 2.5V supply.

The performance of the antennas alone as well as with the LNA present is characterized using a balanced measurement setup consisting of a vector network analyzer, baluns, and balanced probes [3]. Figure 19.6.3b shows the measured transducer gain (18.1°) from 6 to 18GHz between two on-chip dipole antennas separated by 3.9mm. A transducer gain of -64dB is attained at 7.4GHz. Part of the large attenuation is from conduction loss and reflections due to the presence of circuit test structures located between the antennas. These structures contain multiple metal layers, vias, substrate connections, and passivation openings. The measured input impedance at 7.4GHz is approximately 20+j300Ω. This results in ~11dB mismatch loss at 7.4GHz for each antenna, which accounts for ~20dB of the 64dB attenuation.

Figure 19.6.4 shows the measured antenna transducer gain is overlaid for reference in the same figure. Figure 19.6.4b shows the extracted LNA gain. Also shown is a curve fit to this gain as well as the measured S_0 of the LNA. The extracted gain and the measured gain qualitatively agree, demonstrating operation of the integrated antenna/LNA combination.

An 8:1 frequency divider is implemented using three cascaded 2:1 dividers. Each 2:1 divider consists of two source-coupled-logic D-flip-flops in a master-slave configuration [5]. The outputs are tied to the inputs with inverted phase to perform a toggle operation, as shown in Figure 19.6.5. The differential structure detects clock signals with a low voltage swing, increasing the minimum detectable signal of the receiver at a given frequency. The sizing of the transistors limits the output voltage swing, which decreases the power consumption. Measurement results show that the divider operates up to ~10GHz at a 2.5V supply, consuming 18.4mW. For this frequency, an input signal swing of 2.2V_p-p is required, while at 7.4GHz, ~40mV_p-p is required.

Figure 19.6.6 shows plots of the input voltage to the transmitting antenna and the output voltage for the wireless clock receiver, demonstrating the operation of an on-chip wireless interconnect. To overcome the low transducer gain of the antenna pair, the input power level is 21dBm using an external amplifier. The input signal plotted in Figure 19.6.6 is taken before the external amplifier. The input frequency is set to 7.4GHz and the output frequency is 925MHz. The reduced voltage swing at the output is from driving a 50Ω load. Inferring from the measured antenna-pair transducer gain, the received signal level is 43dBm at the LNA input. The receiver consumes 62.5mW from a 2.5V supply. Figure 19.6.7 shows a die photo of the receiver with an integrated dipole antenna. The receiver including the antenna is 0.7x2mm², while the receiver alone is 540x730µm².

Referring to Figure 19.6.3b, increasing the operating frequency to 18GHz improves transducer gain by ~25dB. By optimizing antenna gain and impedance, and using a 0.15- or 0.13µm CMOS process, it should be possible to implement an 18GHz system with greatly improved performance. These early results suggest the possibility of an IC integrating antennas and receivers for inter- and intra-chip wireless interconnection.

References:
[4] Floyd, B. et al., “A 900MHz, 0.8µm CMOS Low Noise Amplifier with 1.2dB Noise Figure,” IEEE CICC, May 1999, pp. 661-664.
Figure 19.6.2: Schematic of LNA and source-follower buffers.

Figure 19.6.3: (a) S-parameters of LNA. (b) Transducer gain of antenna pair.

Figure 19.6.4: (a) Transducer gain of antenna pair and antenna to LNA. (b) Extracted LNA gain and measured LNA gain.

Figure 19.6.5: Schematic of 2:1 frequency divider.

Figure 19.6.6: Input and output waveforms for the 7.4GHz clock receiver.

Figure 19.6.7: Clock receiver die micrograph.