The Feasibility of On-Chip Interconnection using Antennas

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***Abstract*-**The feasibility of integrating antennas and required circuits to form wireless interconnects in foundry digital CMOS technologies has been demonstrated. The key challenges including the effects of metal structures associated with integrated circuits, heat removal, packaging, and interaction of transmitted and received signals with nearby circuits appear to be manageable. Besides, on-chip interconnection, this technology can potentially be applied for implementation of true single chip radio and radar, inter-chip communication systems, RFID tags and others.

Introduction

Scaling of MOS transistor length to below 0.10 μm has made the implementation of CMOS circuits operating at 20 GHz and higher feasible [1]-[4]. In fact, according to the 2003 International Road Map for Semiconductor (ITRS) [5], the cut-off frequency (f_T) and unity maximum available power gain frequency (f_{max}) targets for the year 2015 are ~ 700 GHz. With such transistors, it should be possible to implement RF circuits operating at 200-250 GHz. At 24 GHz, the wavelength of electro-magnetic waves in free space is 12.5 mm and in silicon it is 3.7 mm. This means a quarter wave antenna needs to be only ~ 3 and 0.9 mm in free space and silicon. These in conjunction with the increases of chip sizes to ~ 2 cm x 2 cm have made the integration of antennas for wireless communication possible.

On-chip antennas could potentially be used to relieve the bottleneck associated with global signal distribution inside integrated circuits (IC's). Wireless interconnects using on-chip antennas could lower clock skew [6] and reduce the impact of dispersion (Fig. 1) besides freeing up wiring resources for other uses. On-chip antennas could also be used for data communication among integrated circuits to lower the I/O pin counts, thus reducing the form factor and packaging costs (Fig. 2) [7], as well as for communication within an IC. By incorporating a technique for eliminating the need for an off-chip crystal reference [8] into a transceiver with on-chip antennas [9],[10], a true single chip radio which is small, reliable and easy to use can also be realized. The availability of sensor nodes incorporating such a radio (μ-nodes, Fig. 3) will accelerate the realization of the Smart Dust vision [11].

This paper reviews the status of key technologies required to implement on-chip and inter-chip wireless interconnect

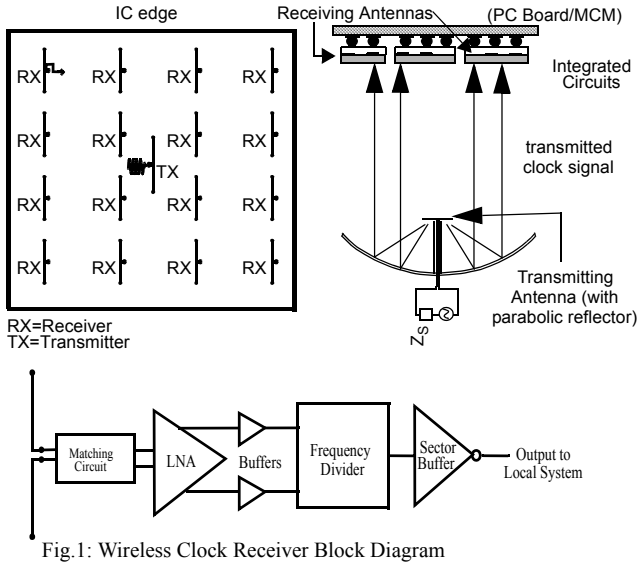

Fig.1: Wireless Clock Receiver Block Diagram

systems as well as challenges and potential solutions. This paper discusses the paths for signal propagation [12], performance of integrated antennas on 10-20 Ω-cm silicon substrates commonly used in CMOS and BiCMOS technologies [13]-[15], circuits which could be implemented in mainstream CMOS technologies for these applications [16],[17] and demonstrations of wireless interconnects [18],[19]. The key challenges including the effects of metal structures associated with integrated circuits [20]-[23], heat removal [18], packaging [19], and interaction of transmitted and received signals with nearby circuits [24]-[27] are discussed.

Figure 4 shows some of the possible paths for signal propagation within an integrated circuit. There are a direct path, a

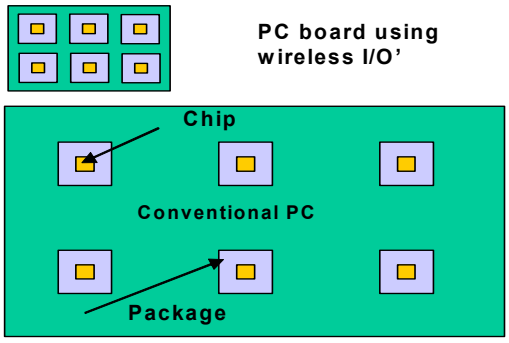

Fig. 2. A printed circuit board with circuits utilizing wireless interconnects.

path formed by refraction through the SiO_2 layer and reflection at the interface between the silicon/underlying dielectric layer (AlN), and a path refracted through the SiO_2 and silicon layers and reflected by the metal chuck which emulates a heatsink in the back of a die. The signals propagating on these paths constructively and destructively interfere. There are also multiple reflected paths. However, due to longer path lengths, the signals propagated on these paths suffer from greater attenuation and these paths are not included.

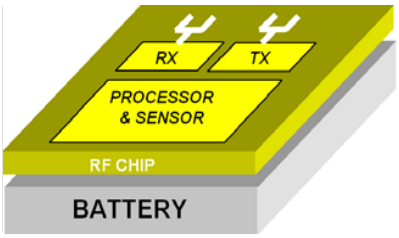

Fig 3, A conceptual diagram of a μ-node.

Fig. 5 shows G_a versus frequency plots for varying thicknesses of AlN layer between the silicon and metal chuck. The measurements were made using a pair of 2-mm zigzag dipole antennas shown in Fig. 6 and the separation between the antennas was 5 mm. The antenna pair power gain, G_a is defined as

$$G_a = \frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 e^{-2\alpha R} \quad (1).$$

G_a includes the gains of transmitting (G_t) and receiving antennas (G_r), and the propagation loss effects in the medium including the conduction loss. λ is the wavelength, α is the attenuation constant which accounts for the substrate conduction loss, and R is the antenna separation. G_a is obtained by measuring the 2-port S-parameters of an antenna pair, and de-embedding the mismatch losses using $|S_{11}|^2$ and $|S_{22}|^2$.

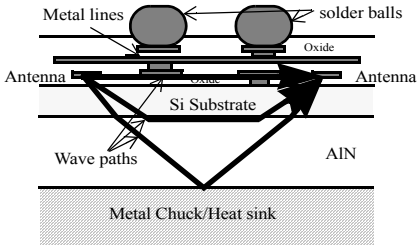

Fig. 4, Some of the possible propagation paths.

The dips due to destructive interference effects are observed in the plots. As the AlN thickness is increased, the frequencies at which the dips occur are lowered. This and the fact that G_a improves when the substrate is made insulating [13],[14] are clear indications that the signal transmission and reception are via wave propagation. The addition of a 0.76-mm thick AlN layer improves the power transmission gain by around ~10 dB compared to the case when the wafer is in direct contact with the metal chuck. The AlN layer has a thermal conductivity comparable to Al and provides an excellent thermal path for heat removal. Fig. 7 shows the radiation patterns of dipole and loop antennas at 10 GHz,

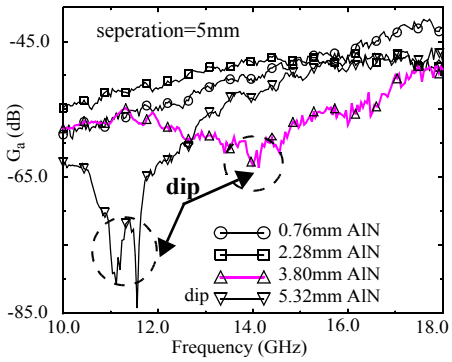

Fig. 5, G_a vs. frequency when the AlN propagating layer thickness is varied.

which are consistent with the basic antenna theory.

As mentioned, clock distribution can be a potential application for on-chip wireless interconnects. In the wireless approach, the clock is transmitted using a monotone sine wave and the received signal is amplified, divided and buffered to locally provide clock signals (Fig. 1). At the 0.18-μm generation, the latency for wireless clock distribution system was estimated to be around ~ 400 pS compared to ~ 1 nS of conventional clock distribution networks. The latencies to all points in a chip must be matched to a tighter tolerance with each generation of technologies to facilitate the increase of clock frequency. The latencies in wireless systems are dominated by the delay through clock receiver circuits and this delay scales down with technology as shown in Fig. 8, while the latency for conventional system is expected to remain essentially constant. This means for conventional clock distribution systems, the latencies must be matched to a smaller percent of the total latency compared to a wireless clock distribution network. Furthermore, for the wireless approach, the clock drivers are distributed over the chip (Fig. 1). This should reduce the temperature variation in the chip, which is a significant source of skew. These are fundamental distinctions that could lead to smaller skew for a wireless clock distribution system. In addition, since a single tone sine wave is used for clock transmission, the dispersion which has been suggested as the effect which could ultimately limit the chip size and clock [28] is greatly reduced.

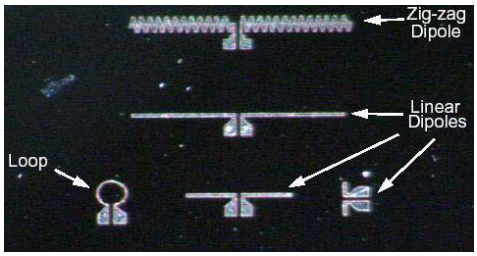

Fig. 6, On-chip antennas fabricated on a 20-Ω-cm substrate.

On wafer, a 15-GHz transmitted signal 2.2 cm away from a clock receiver with an on-chip antenna has been successfully picked up by the receiver and amplified to generate a digital output signal [18] (Fig. 9). The receiver and transmitting antennas were fabricated using a 0.18-μm CMOS process [17]. Fig. 10 shows micro-photographs of the transmitter and receiver. The area including the antenna is 5.86 x 10^5 μm^2. The area excluding bond pads is 3.75 x 10^5 or (~ 600 x 600)

μm^2. The receiver consumes 40 mW of power. For the clock application, transmission over 2.2 cm is sufficient for the largest chip projected by the 2003 ITRS [5].

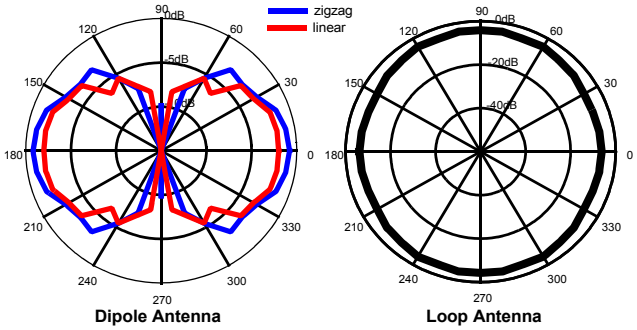

Fig 7, radiation patterns of dipole and loop antennas.

The measured peak-to-peak jitter of receiver is 6.6 ps at 1.875 GHz, corresponding to 1.24% of a local clock period [29]. This is promising, however, to properly evaluate, measurements in IC's with a large number of digital circuits are needed. The power consumption of a wireless clock distribution system using 16 receivers over the areas projected by the ITRS has been estimated and found to be comparable to that of conventional systems [30]. This is due to the fact that most of the power consumption of a clock distribution network is expended for driving local loads.

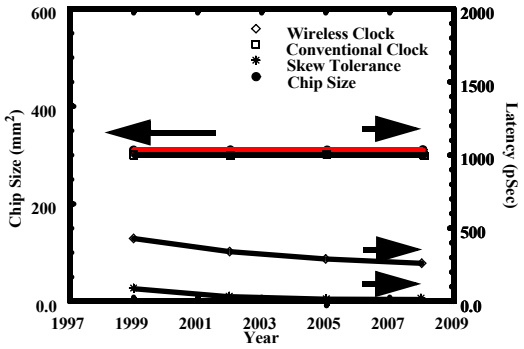

Fig. 8, Latencies versus time for clock distribution systems.

The characteristics of on-chip antennas are expected to be strongly influenced by packaging, and dealing with this has been considered as a major challenge. The chips including the receiver and transmitter shown in Fig. 10 were housed in 407-pin flip-chip packages with a ball grid array (BGA), and tested on a printed circuit (PC) board (Fig. 11) [19]. The relative permittivity of underfill is 3.2. The package is 16 mm x 16 mm with two metal layers. The PCB contains four metal layers, and the dielectric is FR4. The transmitter consists of a voltage controlled oscillator, an amplifier, and an antenna. The transmitter occupies an area of ~600x400 μm^2 excluding the bond pads, and consumes 50 mW of power.

Using these, a sine wave generated in a transmitter was transmitted through an on-chip antenna and the wave was picked up by a receiver in the same chip ~4 mm away. The separation was limited by the size of chip. The testing requires only dc connections to the receiver and transmitter

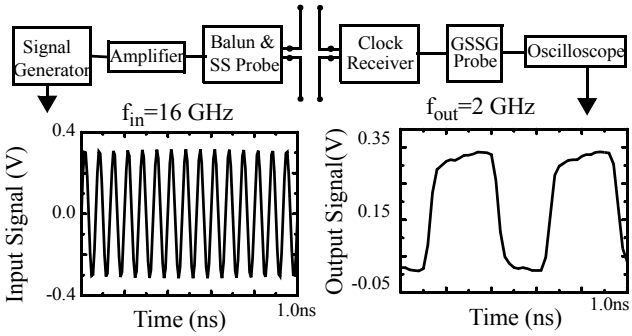

Fig. 9, Transmitted and the digital output signal of a clock receiver 2.2 cm away from the transmitting antenna.

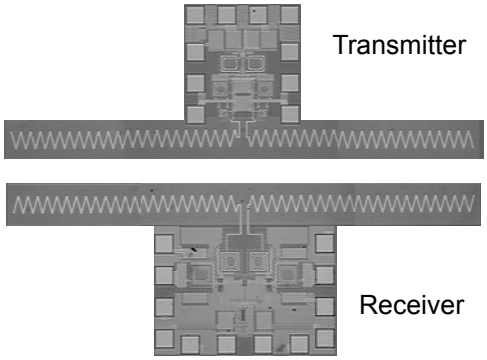

Fig. 10, A transmitter and receiver pair fabricated in a 0.18-µm CMOS process.

except the output connections for the receiver. The output similar to that shown in Fig. 9 has been obtained clearly indicating that on-chip wireless interconnects function even inside a package.

For a clock distribution system with an external planar array antenna (Fig. 12), a clock signal with total skew less than ~14 pS can be provided over an area of 3.8 cm x 3.1 cm [31] in the presence of a heatsink [32]. This should be sufficient for a system operating ~3 GHz. The area is ~4X larger than that typically thought possible for synchronization at such a frequency. Furthermore, the receiving antennas can be significantly shorter than 1 mm [33]. Lastly, the form factor of this system could be comparable to that of conventional systems deployed in desktop computers.

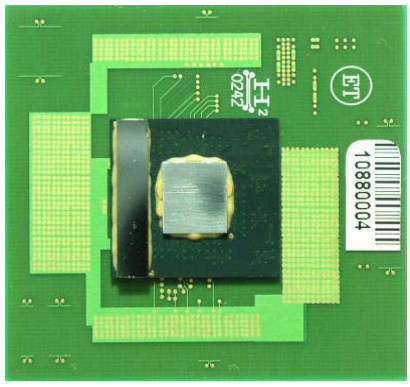

Figure 11, The testchip shown in Figure 10 was packaged in a flip-chip package with a ball grid array. The chip was tested in a printed circuit board.

Metal structures near antennas can change input impedances and phase of received signals. To deal with this,

design guidelines to exclude the interference structures which significantly change the input impedance and techniques to correct the phase changes are being developed [22],[23]. Another concern is the interference effects between transmitted signal and nearby circuits, and between the transmitted/received signal and switching noise of nearby circuits [24]-[27]. A 925-MHz output signal of a 7.4 GHz wireless interconnect [16] is used to drive 100-stage long inverter chains (Fig. 13). This was the first use of a wireless interconnect to drive a digital circuit. As the number of inverter chains is increased, jitter of the received signal increases and ultimately, the receiver fails. The cause for this is the changes in the receiver amplifier gain and self-oscillation frequencies of the frequency divider due to the substrate noise injected from the switching inverters. The operation was restored by increasing the transmitted power to compensate for the gain reduction and by re-centering the self-oscillation frequency of the divider [27]. It should be possible to reduce the sensitivity to the substrate injected noise by using guard rings and a triple n-well process which is starting to be widely available to isolate the body nodes of NMOS transistors in clock receivers.

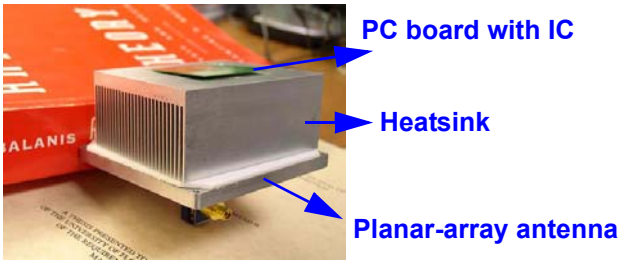

Fig. 12. A compact clock distribution system using an external planar array antenna. A fan could be placed on the sides.

The on-chip antennas can also be used for data communication [6],[34],[35]. The packaging cost not following the silicon die cost reduction curve has been cited as a difficult challenge facing the silicon IC industry beyond 2010 [5]. To alleviate this problem, the input/output (I/O) pins could be replaced with wireless connections formed using transmitters and receivers with on-chip antennas. Transient characteristics of antennas [36] as well as fractal antennas [37] with ultra wide band matching have been investigated for this purpose. Each receiver and transmitter pair can replace multiple pins by use of multiple access techniques such as frequency division multiple access, code division multiple access and others. This decrease of number of pins reduces the foot prints of packaged IC's as conceptually illustrated in Fig. 2. This should also decrease the delays between pins. This delay reduction however, must be balanced by the added delays of transmitter and receiver. The wireless data communication can also provide additional capabilities such as communication by more than one pair of devices at the same time [38].

The two main concerns for inter-chip and intra-chip wireless data communication are the bandwidth and power consumption. The bandwidth is limited by the maximum

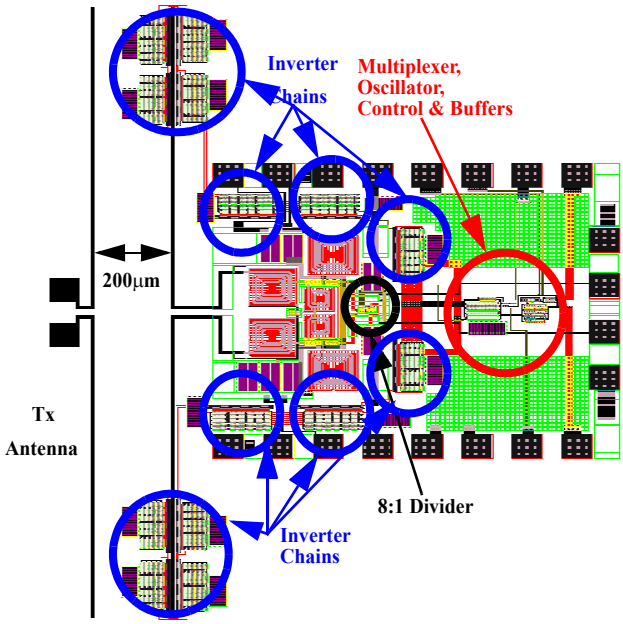

Fig. 13, A 7.4-GHz clock receiver surrounded by inverter chain driven by the receiver.

operating frequency of RF circuits. As discussed, by 2015, RF circuits operating up to ~250 GHz could be fabricated in CMOS technologies. This seemingly high operating frequency by itself will most likely not sufficient to support the required bandwidth for intra-chip and inter-chip data communication. The typical bandwidth efficiency of ~1 bit-sec^{-1}-Hz^{-1} leads to a data rate of only ~250 Gbits/sec. To overcome this, cellular data communication much like that used for cellular phones could be utilized. For instance, if the space around a chip can be divided into 10 cells, this could increase the aggregate data rate to ~2.5 Tbits/sec, which should probably be sufficient for the inter-chip applications in 2015.

For general purpose intra-chip global data communication, the ~2.5-Tbits/sec data rate is still unacceptably low. This however does not preclude the use of on-chip wireless communication for distributing global control signals such as RESET and SLEEP as well as for specialized global and intermediate data communication with moderate bandwidth requirements. For the control signals, it maybe possible to share the antennas and parts of the clock receiver circuitry to reduce the overhead.

Conclusions

It is clear that on-chip antennas can be used to communicate within and between IC's. Signals propagate at the speed of light of a propagation medium [13], but wireless interconnects using on-chip antennas do not require optical components that are difficult to integrate [39]. As the maximum operating frequency of RFCMOS circuits increases with technology scaling, the required antenna and circuit areas will scale down. For example, at 250 GHz, quarter wave antennas for use in air and in silicon will be 300 and 90 μm long, respectively. This will reduce the cost of on-chip wireless interconnects and

greatly increase the flexibility for use of on-chip antennas. The on-chip wireless interconnect technology can potentially be used to increase the clock frequency of digital systems, and to reduce the number of I/O pins and wires in integrated circuits.

Acknowledgements

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