Employing 65 nm CMOS SOI for 60 GHz WPAN Applications

Part 2

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Introduction

• The worldwide 7GHz unlicensed band around 60GHz provides the possibility of multi-gigabit-per-second wireless communication and is a real opportunity for developing next generation wireless personal area networks (WPANs)

• CMOS SOI technology in the nanometer technology node like 65nm offers an alternative to expensive III-V semiconductors

• Developing circuits at MMW frequencies using the 65nm CMOS SOI process is challenging and requires new design methods and flows.

• This presentation will show this new methodology.
Agenda

• Overview of Previous work
  – CMOS SOI 65nm for upcoming WPAN chip sets
  – Modeling for mmWave circuit design
  – 60 GHz transceiver circuit block design

• HFSS CPW component library in Cadence ADE
  – HFSS dynamic link concept
  – Building HFSS dynamic link library in Cadence ADE
  – HFSS dynamic link library validation (with Nexxim)

• Receiver Design
  – VCO+Buffer+Divider
  – LNA+Mixer+IF Amplifier

• Conclusion
Overview of Previous work
60 GHz for WPAN
Application

• 7 GHz unlicensed bandwidth around 60GHz worldwide
  – Australia 59.4-62.9 GHz
  – Canada & USA 57-64 GHz
  – Japan 59-66 GHz
  – Europe 57-66 GHz

• Few regulatory specifications
• Simple modulation scheme for Giga-Bit data rates
• Compact Antennas enable an integrated antenna solution
MMWave design challenges

• 60 GHz is challenging for CMOS Device Performance
  – As freq ↑ Available Gain and Power↓, NF ↑

• Accurate interconnect and passive device models required to characterise loss, Q...

• Unexpected parasitic effects e.g. cross-talk through substrate.

• Chip interconnect issues – flip chip, bond wire etc

• Packaging

• Measurement!
 Passive Component Library

- 3D EM modelling and validation
- Electrical model creation
- Building model card in Spectre format
- Passive component creation for Nexxim
  - Cadence ADE
  - Ansoft Designer
- Passive component library validation

- Varactor_VCO area=18
- CPW_Bend W=5um S=5um TempK=290
- CPW_T_Junction W1=12um W2=12um W3=12um S1=5um S2=5um S3=5um TempK=290
CPW transmission lines 3D
EM modeling

Full 3D Simulation in HFSS as a function of W, G, stackup and frequency (1GHz to 110 GHz)

Extraction of

- $Z_c (\text{Re} & \text{Im})$
- Propagation constant $\gamma (\text{Re} & \text{Im})$

As a function of
- W
- G
- Frequency
CPW electrical modelling for CAD tools

Implementation ABCD matrix description:

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix} = \begin{bmatrix}
\cosh(\gamma L) & Z_c \sinh(\gamma L) \\
\frac{1}{Z_c} \sinh(\gamma L) & \cosh(\gamma L)
\end{bmatrix}
\]

\[
\langle i_n^2 \rangle = 4KT \Re\left(\frac{D}{B}\right)
\]

\[
\text{Cor} = \frac{\Re\left(-\frac{1}{B}\right)}{\Re\left(D/B\right)}
\]

\[
Z_c = M_1 G_{M_2} + M_3 G_{M_4} + M_5 f_{M_6} + M_7 f
\]

\[
\Im(Z_c) = -N_1 f^{K_1} - N_3
\]

\[
\beta = \frac{2\pi f}{C_0} \sqrt{\varepsilon_{\text{eff}}}
\]

\[
\varepsilon_{\text{eff}} = L_4 f^{K_2} + L_5 G^{K_4} + L_6 G + L_0
\]

\[
\gamma = K_1 (G^{K_3}) + K_4 f + K_5 G
\]
Model Validation: Filter Example

- TRL
- Bend
- Tee
- Cross

3D EM Structure (symmetric)
Varactor_VCO
area=18

MOM_25_105
L=LengthCap
60 GHz WPAN Receiver
design building blocks

Variation of 8 GHz

S11 & S22 in dB

S21 in dB

Output Spectrum at Fin = 59GHz
Further work

- Design Buffer to increase sensitivity of the divider
- Design Mixer
- VCO-Buffer-Divider co-design
- LNA-VCO-Mixer co-design
HFSS dynamic link library in Cadence ADE
How to build passive component library

• Analytical model
  – Create parameterized HFSS 3D EM project
  – Run parametric analysis
  – Create a model
  – Extract data from HFSS 3D EM analysis to define model coefficient and build model card
  – Use analytical model in circuit simulation

• HFSS Dynamic Links to Nexxim
  – Create parameterized HFSS 3D EM project
  – Run parametric analysis
  – Directly use HFSS results database in circuit simulation (with Nexxim)
HFSS Dynamic Links overview

- HFSS solution database is linked to Nexxim circuit simulator via dynamic link model
- HFSS variables are mapped to component parameters
- Interpolation of existing solution or simulation of missing solution

Inspiring Engineering
Optimize HFSS project for parametric Analysis
Stackup Simplification for 3D EM Simulation

CMOS Back-end

Multi dielectric layers
SiO₂/Si₃N₄

STI
BOX

Si

Equivalent Back-end for 3D simulations

Passivation

Diel1
Diel2
Diel3

Cu

Al

ε_r(eq) = \left( \frac{\sqrt{\varepsilon_n} + \frac{h_{n-1}}{h_n} \left( \sqrt{\varepsilon_{n-1}} - \sqrt{\varepsilon_n} \right)}{h_{n-1} + h_n} \right)^2
Parameterisation and setup

- Fully parameterized geometry vs. w, gap, stackup
- Use metal to override dielectric option
- Use symmetry plane when possible
- Use Solve Ports Only for transmission line (Dynamic Link TRL model)
- Use de-embedding for discontinuities
HFSS Projects: Transmission Lines

- M1M6-Alucap and M6-Alucap
  - Frequency sweep DC to 110Ghz
  - Extrapolation to DC @ 0.3MHz
  - Solve port only solution
    - Dynamic Links TRL model
    - Reduce simulation time
  - Symmetry plane assigned
  - Parameterization
    - W, Gap, L, Material thickness
  - Analysis
    - W= 12um and w=5um
    - Sweep gap from 2um to 26um with step of 0.5um (98 variations)
    - DSO using 8 cores (Xeon 3GHz double quad core)
    - Simulation time ~20mn
HFSS Projects: Bend and Tee Junction

• Bend and Tee (M6-Alucap)
  – Frequency sweep DC to 110Ghz
  – Extrapolation to DC 0.3MHz
  – Material thickness parameterization
  – Add de-embedding arm of 200um
  – Bend Analysis
    • W=12um and w=5um
    • Sweep gap from 2um to 26um by step of 1um
    • DSO using 8 cores (Xeon 3GHz double quad core) ~ 4h34

• Tee
  • W1, W2, W3, S1, S2, S3 parameterization
  • No parametric analysis for Tee
  • Simulation for one variation with DSO using 8 cores (Xeon 3GHz double quad core) ~ 28mn
Building HFSS Dynamic Links Cadence cell
Nexxim integration in Cadence allows to use Spectre Schematic, Spectre artist_state and Spectre Design kit, then post process results in Cadence after running simulation. User only need to select Nexxim and specifics setting in Nexxim Simulator Control window.
Ansoft specific menu allows to automatically create a cell linked to HFSS project in ANSOFT library.
Use HFSS Dynamic Links Cell in Schematic

- Insert HFSS Dynamic links cell in schematic like standard cell
- HFSS Dynamic links cell can be mixed with standard component from the Design kit
- Use Nexxim to run simulation and get accuracy of 3D HFSS solution data
HFSS Dynamic Links Model Validation
Transmission Line validation

- Loss and Zc as function of stackup and line geometry.
  - M1-M6Al = Full stackup for CPW central line
  - M6-Al = only M6-Al for CPW Central Line
  - HFSS Dynamic Link TRL Model versus Analytical Model

![Graphs showing Alpha in dB/mm vs. gap and Z0 vs. gap for different models with various conditions.](image-url)
Tee and transmission line model validation

- State Space model validation warranties HFSS dynamic Links model to be used in time domain simulation
Stub Filter validation

Stub Filter S11 and S21 in dB vs. Frequency
LNA validation

S21 in dB

S22 in dB

S11 in dB

Curves:
- S21 HFSS Model
- S21 Analytical Model
- S21 Measurements

- S22 HFSS Model
- S22 Analytical Model
- S22 Measurements

- S11 HFSS Model
- S11 Analytical Model
- S11 Measurements

S11 Measurements
Tranceiver Design
Buffer Design
VCO + Buffer Simulation

Adding buffer to VCO allow to increase divider range by 2 GHz
VCO + Buffer + Divider
VCO + Buffer + Divider Simulation

- Divider locked
- Vco period = 2*Divider period

- Divider not locked
- Vco period ≠ 2*Divider period
VCO + Buffer + Divider Simulation

Divider not locked

Red Spectrum: Divider output

Blue Spectrum: VCO output

Divider locked

Divider output wave form

Not locked

Divider output wave form

Locked
LNA + Mixer + IF Amplifier
LNA + Mixer + IF Amplifier

LNA

VCO

IF Amplifier
LNA+ Mixer + IF Amplifier

IF(99.72MHz, -19.85dBm)
LNA+ Mixer + IF Amplifier
Conclusion

- HFSS Dynamic Link
  - HFSS project used as model in Cadence ADE with Nexxim simulator
  - Accuracy validated up to 110GHz against measurements
- Buffer amplifier increased Divider range up to 4GHz
- Simulation of complex sub-block possible with Nexxim in both time and frequency domain